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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,834	06/20/2001	John F. Lane	10821/51085	4115

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EXAMINER	
CORRIELUS, JEAN M	

ART UNIT	PAPER NUMBER
2162	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,834	LANE ET AL.	
	Examiner	Art Unit	
	Jean M. Corrielus	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response the amendment filed on June 26, 2006, in which claims 1, 3, 4 and 10-13 are presented for further examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3, 4 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 26, 2006 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-4 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al., (hereinafter "Van") US Patent no. 5,920,873 and Southgate US Patent no. 6,161,211.

As to claims 1, 14 and 22, Van disclose a design control system usable in a concurrent engineering process to enable the design to be processed. In particular Van discloses the claimed "a library of format readers for reading at least one intelligent design saved in a specific format" by creating a model interactively with user activities (col.12, lines 65-66; col.100, lines 45-57); "a format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format" automatically creating a data structure type for each data design (col.15, lines 10-22; col.19, lines 5-24; col.20, lines 17-18); "an import application-programming interface linked to the format verifier for importing the intelligent design in the applicable format for viewing the intelligent design"importing a located filed by use of an application program interface with a collection of model management utilities (col.7, lines 24-28; col.12, line 66-col.13, line 11); "a memory resident data model, linked to the import application-provamming interface, is a database for storing the properties and functional characteristics of the intelligent design" (col.13, lines 12-16); "a query application-programming interface, linked to the memory resident data model, for searching for at least one element in the memory resident data model" by receiving a request from the displayed client screen to fulfills the request by a providing a result which provides a dynamic way to track a model during the design phase (col.12, lines 55-66); and "a user interface, linked to the query application-programming interface, for interactively accessing the memory resident data model" as an application program interface that provides a control panel input, which allows creation of a

model by interactive user activity and by importing file listings an(col.7, lines 22-28). However, Van does not explicitly disclose an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application. On the other hand, Southgate discloses an analogous system that is directed to software tools for facilitating automated circuit design (col.2, lines 33-38). In particular, Southgate discloses the claimed "an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application" (col.3, lines 23-67; col.4, lines 15-20; col.6, lines 12-24; col.8, lines 32-48; col.9, lines 1-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the design control system library provided therein (see Van.fig.5) would incorporate the use of an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention in a single software application, in same conventional manner as disclosed by Southgate. One having ordinary skill in the art would have found it motivated to use such an automated format verifier of South gate into Van'system because the optimation and mapping processes of Van's system would make better decision, thereby improving the performance and efficiency of optimized routed netlist.

As to claims 3, Van discloses the claimed "at least one format writer, linked to the query application- programming interface, for controlling a local configuration and behavior of the user interface" (col.7, lines 22-30; col.15, lines 10-28).

As to claims 4, Heile discloses the claimed "a collaborative network element, linked by at least one medium to the memory resident data model, for using the apparatus across a global computer network" (col.3, lines 1-8; col.8, lines 20-24, lines 55-66).

As to claims 10, Heile discloses the claimed "wherein the memory resident data model stores a plurality of intelligent designs" (col.8, lines 30-34).

As to claims 11, Heile discloses the claimed "wherein the plurality of intelligent designs have different application formats" (col.6, lines 25-36).

As to claims 12, Heile discloses the claimed "wherein the memory resident data model stores the plurality of intelligent designs in a format that allows simultaneous viewing" (col.5, lines 25-53; col.6, lines 22-55; col.7, lines 23-32; col.17, lines 6-17; lines 30-40).

As to claims 13, Heile discloses the claimed "wherein the memory resident data model provides connectivity between analogous device elements in the plurality of intelligent designs" (col.7, lines 23-33).

6. Claims 1, 3-4 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al., (hereinafter "Van") US Patent no. 5,920,873 and Dole US Patent no. 6,634,008.

As to claims 1, 14 and 22, Van disclose a design control system usable in a concurrent engineering process to enable the design to be processed. In particular Van discloses the claimed "a library of format readers for reading at least one intelligent design saved in a specific format" by creating a model interactively with user activities (col.12, lines 65-66; col.100, lines 45-57); "a format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format" automatically creating a data structure type for each data design (col.15, lines 10-22; col.19, lines 5-24; col.20, lines 17-18); "an import application-programming interface linked to the format verifier for importing the intelligent design in the applicable format for viewing the intelligent design"importing a located filed by use of an application program interface with a collection of model management utilities (col.7, lines 24-28; col.12, line 66-col.13, line 11); "a memory resident data model, linked to the import application-provamming interface, is a database for storing the properties and functional characteristics of the intelligent design" (col.13, lines 12-16); "a query application-programming interface, linked to the memory resident data model, for searching for at least one element in the memory resident data model" by receiving a request from the displayed client screen to fulfills the request by a providing a result which provides a dynamic way to track a model during the design phase (col.12, lines 55-66); and "a user interface, linked to the query application-programming interface, for interactively accessing the memory resident data model" as an application program interface that provides a control panel input, which allows creation of a

model by interactive user activity and by importing file listings an(col.7, lines 22-28). However, Van does not explicitly disclose an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application. On the other hand, Dole discloses an analogous system that is directed to an integrated design environment for the designe and test of integrated circuits. In particular, Dole discloses the claimed "an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention and a single software application" (col.6, lines 53-67; col.8, lines 34-44; col.9, lines 60-67; col.12, lines 58-67; col.14, lines 18-24; col.16, lines 58-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the design control system library provided therein (see Van.fig.5) would incorporate the use of an automated format verifier linked to the format readers for matching the intelligent design to one of the format readers capable of reading the specific format without any user intervention in a single software application, in same conventional manner as disclosed by Dole. One having ordinary skill in the art would have found it motivated to use such an automated format verifier of Dole into Van'system because the optimation and mapping processes of Van's system would make better decision, thereby improving the performance and efficiency of optimized routed netlist.

As to claims 3, Van discloses the claimed "at least one format writer, linked to the query application- programming interface, for controlling a local configuration and behavior of the user interface" (col.7, lines 22-30; col.15, lines 10-28).

As to claims 4, Heile discloses the claimed "a collaborative network element, linked by at least one medium to the memory resident data model, for using the apparatus across a global computer network" (col.3, lines 1-8; col.8, lines 20-24, lines 55-66).

As to claims 10, Heile discloses the claimed "wherein the memory resident data model stores a plurality of intelligent designs" (col.8, lines 30-34).

As to claims 11, Heile discloses the claimed "wherein the plurality of intelligent designs have different application formats" (col.6, lines 25-36).

As to claims 12, Heile discloses the claimed "wherein the memory resident data model stores the plurality of intelligent designs in a format that allows simultaneous viewing" (col.5, lines 25-53; col.6, lines 22-55; col.7, lines 23-32; col.17, lines 6-17; lines 30-40).

As to claims 13, Heile discloses the claimed "wherein the memory resident data model provides connectivity between analogous device elements in the plurality of intelligent designs" (col.7, lines 23-33).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean M. Corrielus whose telephone number is (571) 272-4032. The examiner can normally be reached on 10 hours shift.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean M Corrielus
Primary Examiner
Art Unit 2162

September 13, 2006